UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,195	08/06/2003	Ki-Nam Kim	5649-1130	8323

20792 7590 05/17/2004

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
GARCIA, JOANNIE A	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,195	KIM ET AL.	
	Examiner	Art Unit	
	Joannie A García	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-17 and 20-33* is/are rejected.

7)☒ Claim(s) *14,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 2, 11, and 20-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, line 2, "layer" after "hard mask" should be deleted.

In claim 11, line 4, "lower" before "electrode layer" should be replaced with --first--.

In claim 11, line 6, "electrode" should be followed by --layer--.

In claim 20, line 6, "a" before "semiconductor" should be replaced with --the--.

In claim 32, line 3, "ferroelectric" should be followed by --capacitor--.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5-11, 13, 15, and 16, are rejected under 35 U.S.C. 102(e) as being anticipated by Kotani (US 2003/0038323 A1).

Regarding claim 1, Kotani discloses forming a semiconductor element 2, which could be a capacitor structure on a portion of a substrate 50 including forming a first electrode on the substrate, forming a capacitor dielectric on the first electrode, forming a second electrode on the

dielectric, and forming a hard mask 4 on the second electrode (Figure 7, and Paragraphs 0046, and 0094), so that the capacitor dielectric is between the first and second electrodes (Figure 7), so that the first electrode and the capacitor dielectric are between the second electrode and the substrate (Figure 7), and so that the first and second electrodes and the capacitor dielectric are between the hard mask and the substrate (Figure 7), forming an interlayer dielectric layer 20 on the hard mask and on portions of the substrate surrounding the capacitor structure (Figure 7, and Paragraph 0067), removing portions of the interlayer dielectric layer to expose the hard mask while maintaining portions of the interlayer dielectric layer on portions of the substrate surrounding the capacitor structure (Figure 8A, and Paragraph 0068), and removing the hard mask thereby exposing portions of the second electrode while maintaining the portions of the interlayer dielectric layer on portions of the substrate surrounding the capacitor (Figures 9A-10B, Paragraph 0070, and Paragraph 0073).

Regarding claim 2, Kotani discloses, after removing the hard mask, forming a plate line 29 on the exposed portions of the second electrode (Figure 10B).

Regarding claims 5 and 6, Kotani discloses removing portions of the interlayer dielectric layer 20 comprises planarizing using a CMP process to a level of the hard mask 4 (Figure 8A, and Paragraph 0068).

Regarding claims 7 and 10, Kotani discloses that the interlayer dielectric 20, the hard mask 4, and the second electrode of the semiconductor element comprise different materials, such as, oxide, silicon nitride, and conductive materials, respectively (Figure 7, and Paragraphs 0046, and 0094).

Regarding claims 8 and 9, Kotani discloses removing the hard mask 4 using a phosphoric etchant that selectively etches the hard mask with respect to the interlayer dielectric and the second electrode (Figure 9A, and Paragraphs 0047, and 0070).

Regarding claim 11, Kotani discloses forming a first electrode layer on the substrate 50 (Figure 1A, and Paragraph 0094), forming a dielectric layer on the first electrode layer opposite the substrate (Figure 1A, and Paragraph 0094), forming a second electrode layer on the dielectric layer opposite the first electrode layer (Figure 1A, and Paragraph 0094), forming a hard mask layer on the second electrode layer opposite the dielectric layer, the first electrode layer, and the substrate (Figure 1A, and Paragraph 0094), patterning the hard mask layer to provide the hard mask 4 on the second electrode layer (Figure 1A), and etching portions of the second electrode layer, the dielectric layer, and the first electrode layer using the hard mask 4 as an etching mask to provide the first electrode, the capacitor dielectric, and the second electrode (Figure 3B, and Paragraph 0052).

Regarding claim 13, Kotani discloses forming the hard mask to a thickness of 180 nm (Paragraph 0046).

Regarding claim 15, Kotani discloses forming the interlayer dielectric layer comprising silicon oxide (Paragraph 0046).

Regarding claim 16, Kotani discloses, prior to forming the interlayer dielectric layer 20, forming a hydrogen barrier layer 12/16 on the capacitor structure including the hard mask, the first and second electrodes, and the capacitor dielectric (Figures 4A, and 5B, Paragraph 0094).

Claim 3, 4, 12, 17, and 20-33, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kotani as applied to claims 1, 2, 5-11, 13, 15, and 16 above, and further in view of Kim (U.S. Patent 6,020,233), and Koo (U.S. Patent 6,376,325).

Kotani discloses forming a lower interlayer dielectric 1 on a semiconductor substrate 50 (Figure 1A), sequentially stacking a capacitor structure, and a forming a hydrogen barrier layer 12/16 on the capacitor structure including the hard mask, the first and second electrodes, and the capacitor dielectric (Figures 4A, and 5B, Paragraph 0094). 180 nm silicon nitride hard mask pattern 4 on the lower interlayer dielectric (Figure 1A, and Paragraphs 0046, and 0094), forming a hydrogen barrier layer 12/16 on the capacitor structure including the hard mask, the first and second electrodes, and the capacitor dielectric (Figures 4A, and 5B, Paragraph 0094), forming an oxide inter-metal dielectric 20 to cover an entire surface of the semiconductor substrate including the hard mask pattern (Figure 7), planarizing the inter-metal dielectric layer to expose the hard mask pattern by using a CMP process (Figure 8A), selectively removing the exposed hard mask pattern to expose a top surface of the capacitor structure (Figure 9A-10B), and forming a plate line 29 contacting with the top surface of the capacitor structure (Figure 10B).

Kotani discloses sequentially stacking a lower electrode layer on the substrate 50 (Figure 1A, and Paragraph 0094), a capacitor dielectric layer (Figure 1A, and Paragraph 0094), an upper electrode layer (Figure 1A, and Paragraph 0094), and a hard mask layer on the lower interlayer dielectric layer (Figure 1A, and Paragraph 0094), patterning the hard mask layer to form a hard mask pattern 4 (Figure 1A), using the hard mask pattern as a mask, patterning the upper electrode layer, the capacitor dielectric layer, and the lower electrode layer to sequentially form a lower electrode, a capacitor dielectric pattern, and an upper electrode (Figure 3B, and Paragraph

0052). Kotani discloses selectively removing the hard mask pattern 4 using a phosphoric etchant recipe having an etch selectivity with respect to the inter-metal dielectric and capacitor dielectric (Figure 9A, and Paragraphs 0047, and 0070).

Kotani does not teach forming said capacitor dielectric of a ferromagnetic material consisting of PZT, SBT, and/or BLT, forming said first and second electrodes of materials consisting of ruthenium, platinum, iridium, rhodium, osmium, and/or oxides, and forming said hydrogen barrier layer 12/16 of a material consisting of titanium oxide, aluminum oxide, zirconium oxide, and cerium oxide.

Kim discloses forming a capacitor structure on a portion of a substrate 204, the capacitor structure including a platinum first electrode 230 on the substrate (Figure 4A, and Column 3, line 62), a capacitor dielectric 250 on the first electrode comprising a ferroelectric material such as PZT (Figure 4A, and Column 4, lines 35-37), a platinum second electrode 217 on the dielectric (Figure 4A, and Column 5, line 32), and a hard mask 251 on the second electrode so that the capacitor dielectric is between the first and second electrodes (Figure 4A), so that the first electrode and the capacitor dielectric are between the second electrode and the substrate (Figure 4A), and so that the first and second electrodes and the capacitor dielectric are between the hard mask and the substrate (Figure 4A).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Kotani and Kim to enable formation of the capacitor dielectric, and the first and second electrodes of Kotani to be performed by employing the ferroelectric and electrode materials disclosed by Kim.

Koo discloses forming a capacitor structure including forming a first electrode 122a/124a on a substrate 100 (Figure 4), forming a capacitor dielectric 126a on the first electrode (Figure 4), forming a second electrode 128a/130a on the dielectric (Figure 4), and, prior to forming a interlayer dielectric layer 134, forming a hydrogen barrier layer 132a on the capacitor structure, wherein said hydrogen barrier layer could be made of titanium oxide or aluminum oxide (Figure 4, and Column 6, lines 54-65).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Kotani and Koo to enable formation of the hydrogen barrier layer 12/16 of Kotani to be performed by employing either of the hydrogen barrier materials disclosed by Koo.

Claims 14, 18, and 19, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956 until 2/4/04. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Joannie Adelle García whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 872-9317. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

George Fourson
Primary Examiner
Art Unit 2823

JAG
May 7, 2004

George Fourson
Primary Examiner
Art Unit 2823
(571) 272-1860